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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/631,939
Filing Date: July 31, 2003
Appellant(s): CHAUVEL ET AL.

Utpal D. Shah, Reg. No. 60,047
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 11/16/2007 appealing from the Office action mailed 8/17/2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

Feierbach et al. (U.S. 6,088,786), Seal et al. (U.S. 6,965,984), Kloth (U.S. 6,549,961), and Evoy et al. (U.S. 5,951,689) are relied upon as evidence.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Maintained Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 5-7, 10-11, 14, 17, 20-21, and 23 are rejected under 35 U.S.C. §103(a) as being unpatentable over Feierbach et al. (U.S. 6,088,786), in view of Seal et al. (U.S. 6,965,984), in view of Kloth (U.S. 6,549,961).

3. As per claim 1:

Feierbach disclosed a system, comprising:

A first processor (Feierbach: Figure 2 element 204, column 6 lines 53-67 continued to column 7 lines 1-7);

A second processor coupled to the first processor, the second processor having a core and comprising stack storage residing in the core (Feierbach: Figure 2 elements 104 and 210, column 6 lines 53-67 continued to column 7 lines 1-7);

Memory coupled to, and shared by, the first and second processors (Feierbach: Figure 2 element 212, column 6 lines 53-65)(The data cache is shared by the two processors.); and

A synchronization unit coupled to the first and second processors, said synchronization unit synchronizes the execution of the first and second processors

(Feierbach: Figure 4 element 402, column 10 lines 25-55)(The copy unit monitors data accesses and ensures that data is properly exchanged between processors and other memory units. Thus having the same functionality.);

Wherein the second processor executes stack-based instructions (Feierbach: Figure 2 element 202, column 6 lines 53-65) while the first processor executes one or more tasks (Feierbach: Column 6 lines 21-29)(Feierbach incorporates by reference Yung (U.S. 5,996,066))(Yung: Figure 1, column 3 lines 20-67) wherein the first processor manages the memory via an operating system that executes only on the first processor (Feierbach: Column 6 lines 21-29)(Feierbach incorporates by reference Yung (U.S. 5,996,066))(Yung: Figure 1 elements 44a-b, column 3 lines 20-67)(Yung manages memory through the hardware memory management units. An operating system manages memory through software. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention that the processor of Yung could have managed memory from software using an operating system instead of hardware using the memory management units.) and the second processor executes a virtual machine that controls the execution of a program on the second processor (Feierbach: Column 6 lines 13-21)(Feierbach incorporates by reference Tremblay et al. (U.S. 6,021,469))(Tremblay: Figure 1 element 100, column 5 lines 35-54)(The stack processor runs a virtual machine that controls the execution of instructions.).

Feierbach failed to teach the first processor executes a virtual machine that controls the execution of a program on the second processor; wherein the first processor executes a transaction targeting a pre-determined address and the

synchronization unit detects said pre-determined address and asserts a wait signal to cause said first processor to enter a reduced power or reduced performance mode; and wherein said second processor asserts a wait release signal that is received by said synchronization unit and that causes said synchronization unit to deassert said wait signal to the first processor.

However, Seal disclosed the first processor executes a virtual machine that controls the execution of a program on the second processor (Seal: Figure 18 element 326, column 16 lines 38-48; Figure 20, column 17 lines 38-67)(The processor includes a virtual machine to execute Java bytecodes. Some of the instructions can't be run on the processor, and are executed by software. Thus having the same functionality.).

An advantage of having the first processor process Java bytecodes through acceleration techniques is that the instructions will run faster on the hardware as opposed to the software executing the instructions (Seal: Column 1 lines 19-47). The instructions that are too complex to be executed on hardware are sent off to be executed on software (Seal: Column 1 lines 19-47). One of ordinary skill in the art would have been motivated to use a virtual machine to assist in accelerating Java bytecode instructions for the benefit of increased performance from the accelerated instructions being executed in hardware. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to add a virtual machine to help accelerate Java bytecodes for the advantage of increased performance.

Feierbach and Seal failed to teach wherein the first processor executes a transaction targeting a pre-determined address and the synchronization unit detects

said pre-determined address and asserts a wait signal to cause said first processor to enter a reduced power or reduced performance mode *and* wherein said second processor asserts a wait release signal that is received by said synchronization unit and that causes said synchronization unit to deassert said wait signal to the first processor.

However, Kloth disclosed wherein the first processor executes a transaction targeting a pre-determined address and the synchronization unit detects said pre-determined address and asserts a wait signal to cause said first processor to enter a reduced power or reduced performance mode (Kloth: Figure 2 elements 42, 44, and 48, column 3 lines 51-67 continued to column 4 lines 1-15)(When the first processor requests an unavailable resource, the processor suspends all execution while the halt signal is asserted. This causes the first processor accessing the unavailable resource to have reduced performance from stalling execution.).

Wherein said second processor asserts a wait release signal that is received by said synchronization unit and that causes said synchronization unit to deassert said wait signal to the first processor (Kloth: Figure 3 elements 60, 62, 66, and 68, column 4 lines 16-32)(The second processor that is using the protected resource sends a release signal to the first processor being stalled. Figure 1, element 24 acts as the synchronization unit that stores the semaphores for the processors.).

The advantage of using semaphores is that they are able to resolve resource conflicts between processors (Kloth: Column 1 lines 20-30). One of ordinary skill in the art would have been motivated by this advantage to implement semaphores in the processor of Feierbach and Seal. Thus, it would have been obvious to one of ordinary

skill in the art at the time of the invention to implement semaphores for the advantage of resolving resource conflicts.

4. As per claim 2:

Feierbach, Seal, and Kloth disclosed the system of claim 1 wherein the second processor comprises an internal data memory that holds a contiguous block of memory defined by an address stored in a register, and wherein local variables are stored in said data memory (Feierbach: Column 6 lines 13-21)(Feierbach incorporates by reference Tremblay et al. (U.S. 6,021,469))(Tremblay: Figure 4a-b, columns 9-11).

5. As per claim 5:

Feierbach, Seal, and Kloth disclosed the system of claim 1 wherein the stack-based instructions comprise Java bytecodes (Feierbach: Column 5 lines 4-29) and the first processor comprises a RISC processor (Seal: Figure 10 element 12, column 5 lines 60-67 continued to column 6 lines 1-9) so that the RISC processor executes one or more tasks while the second processor executes Java code.

6. As per claim 6:

Feierbach, Seal, and Kloth disclosed the system of claim 1 further including a main stack residing outside the second processor's core and coupled to the stack storage in the second processor's core (Feierbach: Figure 2 element 212, column 7 lines 8-18).

7. As per claim 7:

Feierbach, Seal, and Kloth disclosed the system of claim 6 wherein the stack storage in the second processor's core provides an operand to execute a stack-based

instruction in the second processor (Feierbach: Figure 2 element 210, column 7 lines 50-65).

8. As per claim 10:

Claim 10 essentially recites the same limitations of claim 1. Therefore, claim 10 is rejected for the same reasons as claim 1.

9. As per claim 11:

Claim 11 essentially recites the same limitations of claim 2. Therefore, claim 11 is rejected for the same reasons as claim 2.

10. As per claim 14:

Claim 14 essentially recites the same limitations of claims 6-7. Therefore, claim 14 is rejected for the same reasons as claims 6-7.

11. As per claims 17:

Claim 17 essentially recites the same limitations of claim 1-2. Therefore, claim 17 is rejected for the same reasons as claim 1-2.

12. As per claim 20:

Feierbach, Seal, and Kloth disclosed the system of claim 1 wherein a clock internal to the first processor is disabled thereby effectuating the reduced power or reduced performance mode (Kloth: Figure 2 element 48, column 4 lines 3-15)(When the first processor requests an unavailable resource, the processor suspends all execution while the halt signal is asserted. This causes the first processor accessing the unavailable resource to reduce performance from stalling execution. Official notice is

given that while the processor is in a wait state, the clock could be gated with the wait signal to disable the clock which results in a reduced power mode.).

13. As per claim 21:

Feierbach, Seal, and Kloth disclosed the system of claim 1 wherein said wait signal remains asserted until said synchronization unit deasserts said wait signal (Kloth: Figure 3 element 68, column 4 lines 16-32)(The second processor that is using the protected resource sends a release signal to the first processor being stalled. Figure 1, element 24 acts as the synchronization unit that stores the semaphores for the processors).

14. As per claim 23:

Feierbach, Seal, and Kloth disclosed the system of claim 17 wherein said synchronization unit continues to assert said first signal until either the synchronization unit receives said second signal from the second processor or the synchronization unit receives an interrupt signal (Kloth: Figure 3 element 68, column 4 lines 16-32)(The second processor that is using the protected resource sends a release signal to the first processor being stalled. Figure 1, element 24 acts as the synchronization unit that stores the semaphores for the processors).

15. Claims 22 and 24 are rejected under 35 U.S.C. §103(a) as being unpatentable over Feierbach et al. (U.S. 6,088,786), in view of Seal et al. (U.S. 6,965,984), in view of Kloth (U.S. 6,549,961), further in view of Evoy et al. (U.S. 5,951,689).

16. As per claim 22:

Feierbach, Seal, and Kloth disclosed the system of claim 1.

Feierbach, Seal, and Kloth failed to teach wherein said second processor asserts said wait release signal when said second processor requires support from said first processor.

However, Evoy disclosed wherein said second processor asserts said wait release signal when said second processor requires support from said first processor (Evoy: Figure 1 element 39, column 3 lines 29-36 and lines 60-67 continued to column 4 lines 1-7)(Element 39 allows for the processor functional units to be in high or low performance mode. Element 39 is in high performance mode when extra functional units are needed to deliver higher performance for an application. It would have been obvious to one of ordinary skill in the art at the time of the invention that this could also be applied to a multiprocessor system in order to turn on and off processors when they are needed and when they aren't needed.).

The advantage of a power control system is that it will allow for slower performance and power savings when an application isn't in need of high performance (Evoy: Column 1 lines 35-49). One of ordinary skill in the art would have been motivated by this advantage to implement power control for the multiprocessor system of Kloth to enable processors to be shut off to save power when they weren't needed. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a power control unit to regulate which processors are turned on and which are turned off for the advantage of power savings when processors aren't needed.

17. As per claim 24:

The additional limitation(s) of claim 24 essentially recite the additional limitation(s) of claim 22. Therefore, claim 24 is rejected for the same reason(s) as claim 22.

(10) Response to Argument

18. Regarding claims 1-2, 5-7, 10-11, 14, 17, 20-21, and 23 are rejected under 35 U.S.C. §103(a) as being unpatentable over Feierbach et al. (U.S. 6,088,786), in view of Seal et al. (U.S. 6,965,984), in view of Kloth (U.S. 6,549,961):

A.) Applicant argues in section A "Feierbach failed to teach a multi-entry stack contained within the core and usable in at least a stack-based instruction set and comprising a plurality of entries and a plurality of registers contained in said core and coupled to the logic and addressable through a second instruction set that provides register-based and memory-based operations. Feierbach is silent to a second instruction set that provides register-based and memory-based operations ... In accordance with Feierbach the extended instructions are one of two "types" of instructions that are part of one set of stack based operations."

The examiner disagrees for the following reasons. Applicant's argument is that the extended stack instructions are part of a single instruction set of Feierbach. The examiner will rebut the appellant's arguments first with a definition of instruction set.

Instruction set is a list of all instructions that a processor can execute. The appellant claims to have a processor with two instruction sets, which might seem to go

against this definition. However, a processor can have multiple cores of execution that execute different types of instructions, with each core executing a single instruction set. Each core executes a separate instruction set because each core was originally designed to execute a specific set of instructions. In addition, the instruction sets can overlap in functionality since each processor core is specifically designed to execute a particular set of instructions. The claimed invention allows for such overlap since it doesn't declare no overlap can occur.

Feierbach disclosed two such processor cores by elements 202 and 204 of figure 2. These elements are two processor cores that are capable of executing two separate instruction sets since each processor core was specifically designed to execute a set of instructions. Feierbach disclose in column 5 lines 62-67 continued to column 6 lines 1-7 that stack instructions are executed as the first instruction set on processor core element 202 and that extended instructions are executed primarily as register-based instructions on processor core element 204. Thus, Feierbach, in view of the definition of instruction set, clearly disclosed two separate instruction sets in elements 202 and 204 of figure 2.

B.) Applicant argues in section A "The office action relies on Feierbach's stack processor for the claimed second processor that "executes stack-based instructions"; however, in paraphrasing the claim the Office action misquotes the claim to be "the second processor executes a virtual machine that controls the execution of a program on the second processor," and then the Office action relies on Feierbach's stack processor as the processor that executes the virtual machine."

The examiner notes that the appellant is incorrect in their assertion that the examiner uses Feierbach to teach a first processor that executes the virtual machine. The examiner is only pointing out that the second processor (element 202) in Feierbach happens to execute a virtual machine, but failed to show the first processor (element 204) executing a virtual machine. The examiner uses different prior art, being Seal et al., that the appellant failed to argue in the appeal brief.

C.) Applicant argues in section A "Kloth failed to teach wherein the first processor executes a transaction targeting a pre-determined address and the synchronization unit detects said pre-determined address and asserts a wait signal to cause said first processor to enter a reduced power or reduced performance mode ... Stated otherwise, Kloth teaches a system where the requesting processor is halted by the bridge; but, the trigger for halting the requesting processor is the data within the data access request sent over the processor bus and unavailability of the requested resource."

The examiner disagrees for the following reasons. The examiner wants to reiterate that the protected resources in the system of Kloth are data being requested by processors. This data is stored in memory, inherently at a pre-determined address. Load and store instructions are used to access memory, and target pre-determined addresses in memory to load/store data. The load/store instructions are the transactions targeting a pre-determined address. In figure 2 elements 44 and 48, it's determined that data being requested by a processor is in use by another processor, which results in the processor being stalled. The stalling of a processor results in no

useful work being performed and results in a reduced performance mode. Thus, Kloth correctly reads upon the claimed limitation.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/JAP/

/Jacob A. Petranek/

January 23, 2008

Conferees:

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